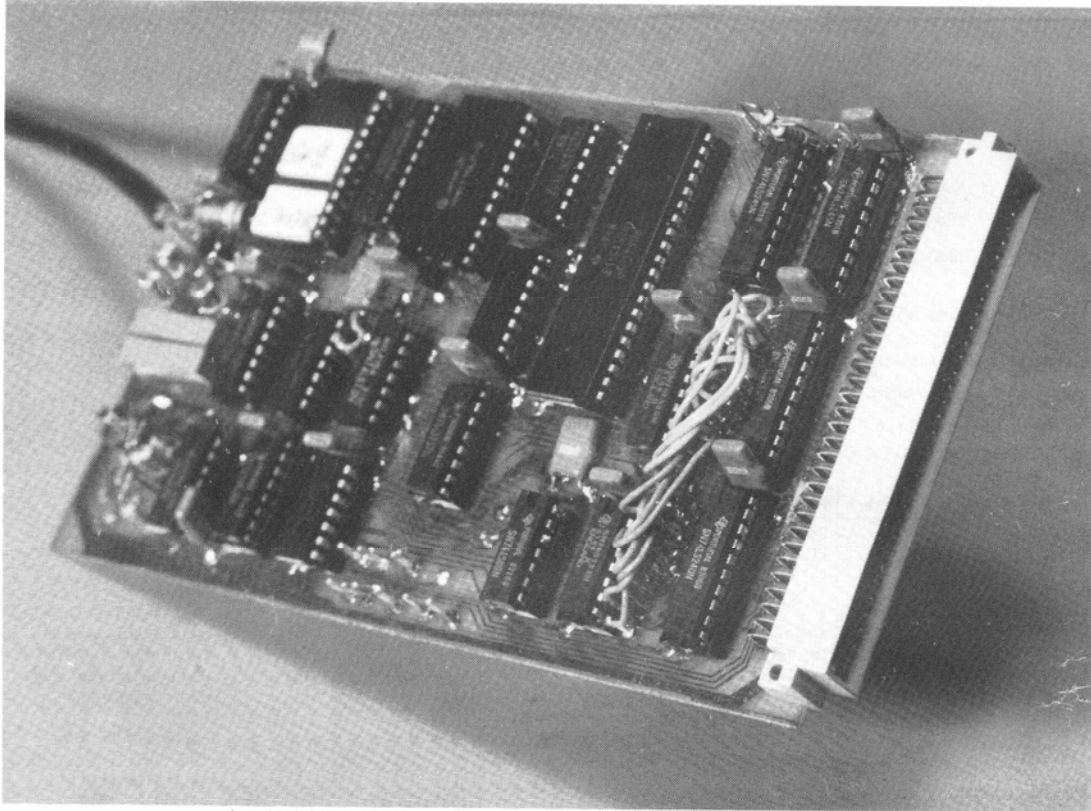# VDU card

In Elektor we like to keep up to date, and we feel that the time has come for a new video card. The VDU card described here is not simply a modern receiver for the old and still popular Elekterminal, rather it is a new design intended to use all the possibilities of a modern computer. It can display 24 lines of 80 characters on the screen, graphics are available, and there are several other possibilities. Numerous Junior Computer users have long been waiting to be able to equip their computer system with its own video card. However, this card is intended not only for the Junior but also for other processors, such as the 6800 family and the Z80.

video for computers

in conjunction with
H. Vermeulen

The accompanying article in this issue 'Video graphics' describes the principles of a VDU card and is good background material for anybody who is not totally familiar with the subject, so, rather than duplicate any of that here, we will simply describe the circuit for the VDU card. At the same time, we must explain what the further possibilities of this card are and this is where we will begin.

VDU card . . . and terminal?

Here we will consider the VDU card as an independent unit. In this form it can be connected directly to the expansion bus of the Junior Computer. The only extra component needed is a 2716 EPROM with a VDU output program in place of the printer monitor program.

Figure 1 shows the main components which make up the VDU. First is the actual VDU card, with the Cathode Ray Tube Controller (6845), a 2 K video RAM (6116), and the character generator — the block diagram is shown in the descriptive article. The character generator consists of a 2732 EPROM in which all the ASCII and graphics symbols are stored in the appropriate dot-matrix

layout (incidentally, graphics are possible by means of 'poke' commands, but we will return to that later). The card can be connected via a 75 Ω video output to a monitor. A connection for a light pen is also included on the card but no software for this purpose has been given in this basic version. It will be a simple matter to incorporate this at a later date. The diagram also shows the 2716 which contains the video routines for the Junior.

The standard format on the screen is 24 lines of 80 characters and because of the bandwidth required, a proper monitor or a TV set with a video input (not the normal aerial input) is needed.

The card also has an interface to adapt the VDU board for a Z80 processor. Similarly, other 6502 computers can be connected to it, as can the 6800 family. Because complete address decoding is possible on the card it can be adapted to practically every modern computer with one of the processors mentioned; AIM 65, SYM, VIC 20, VIC 64 and so on. One thing to remember is that the VDU card uses the Elektor bus and if it is to be used with other systems, the user will have to work out the connections and video routines himself.
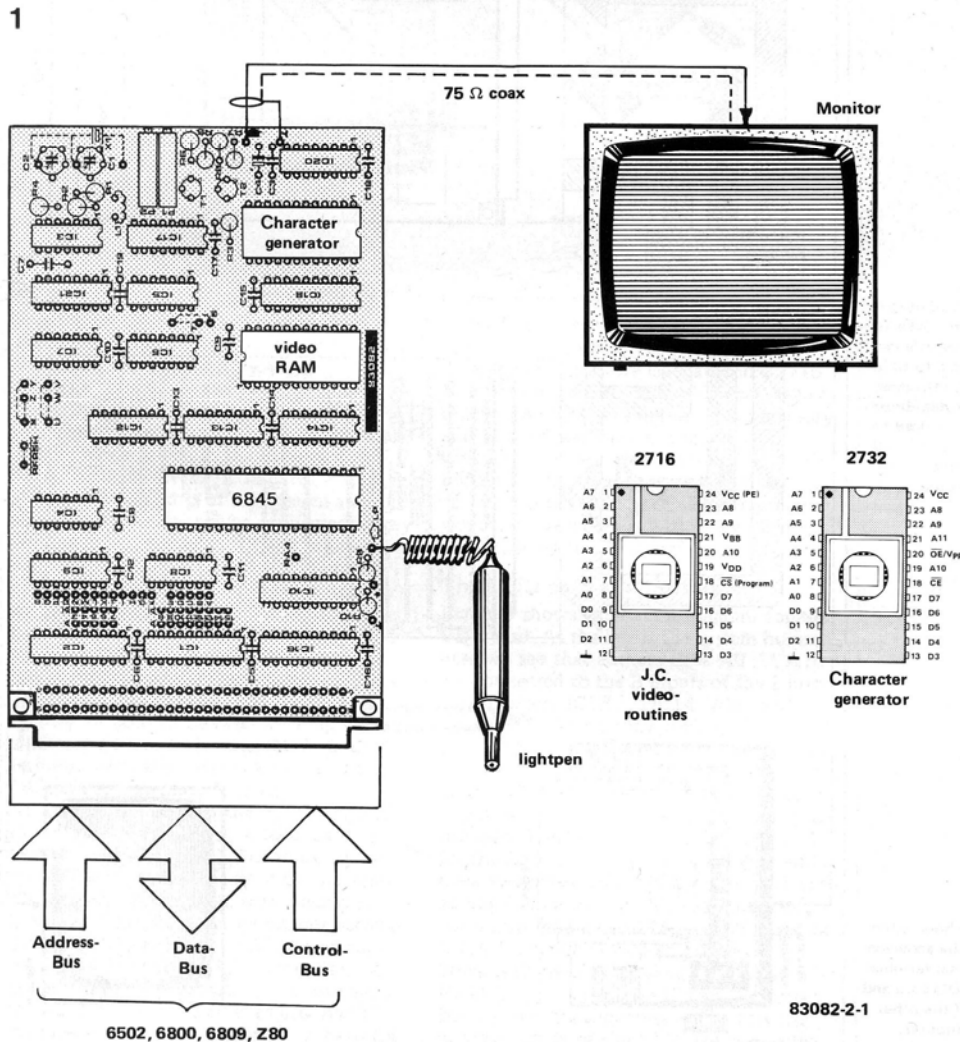
The composite video signal produced by the VDU card can be fed into any monitor. Both the synchronization pulses and the contrast can be adjusted. The whole image can also be inverted to provide black characters on a light background. The cursor can be made to flash or light continuously. The VDU card can be used with the oscillator containing C1, C2 and L1, or these components can be replaced by a 15 MHz crystal, as shown dotted in the circuit diagram. If this is done the image on the screen will be rock steady.

The card is slightly unusual in that all the timing on the card works with synchronously clocked TTL switching. The advantage of this is that no timing faults can occur, even with this high frequency.

As you can see there are already quite a few

Figure 1. This is a sketch of the major components of the VDU card.

1

75 Ω coax

Monitor

Character generator

video RAM

6845

lightpen

2716		2732	
A7	1 • 24 Vcc (PE)	A7	1 • 24 Vcc
A6	2 23 A8	A6	2 23 A8
A5	3 22 A9	A5	3 22 A9
A4	4 21 Vᴮᴮ	A4	4 21 A11
A3	5 20 A10	A3	5 20 ŌĒ/Vpp
A2	6 19 V_DD	A2	6 19 A10
A1	7 18 C̄S̄ (Program)	A1	7 18 C̄Ē
A0	8 17 D7	A0	8 17 D7
D0	9 16 D6	D0	9 16 D6
D1	10 15 D5	D1	10 15 D5
D2	11 14 D4	D2	11 14 D4
⏚	12 13 D3	⏚	12 13 D3

J.C. video-routines

Character generator

Address-Bus   Data-Bus   Control-Bus

6502, 6800, 6809, Z80

83082-2-1

2

Keyboard

parallel
keyboard output

Host
computer

telephone line

Modem

16 bit
computer

programmable
switches

RS 232

RS 232 (VT 52)

VIA

VIA

ACIA

Control-Bus

Data-Bus

Address-Bus

CPU

5564

2732
EPROM

6502

Elektor
bus

VDU

6845

video
RAM

Char.
gen.
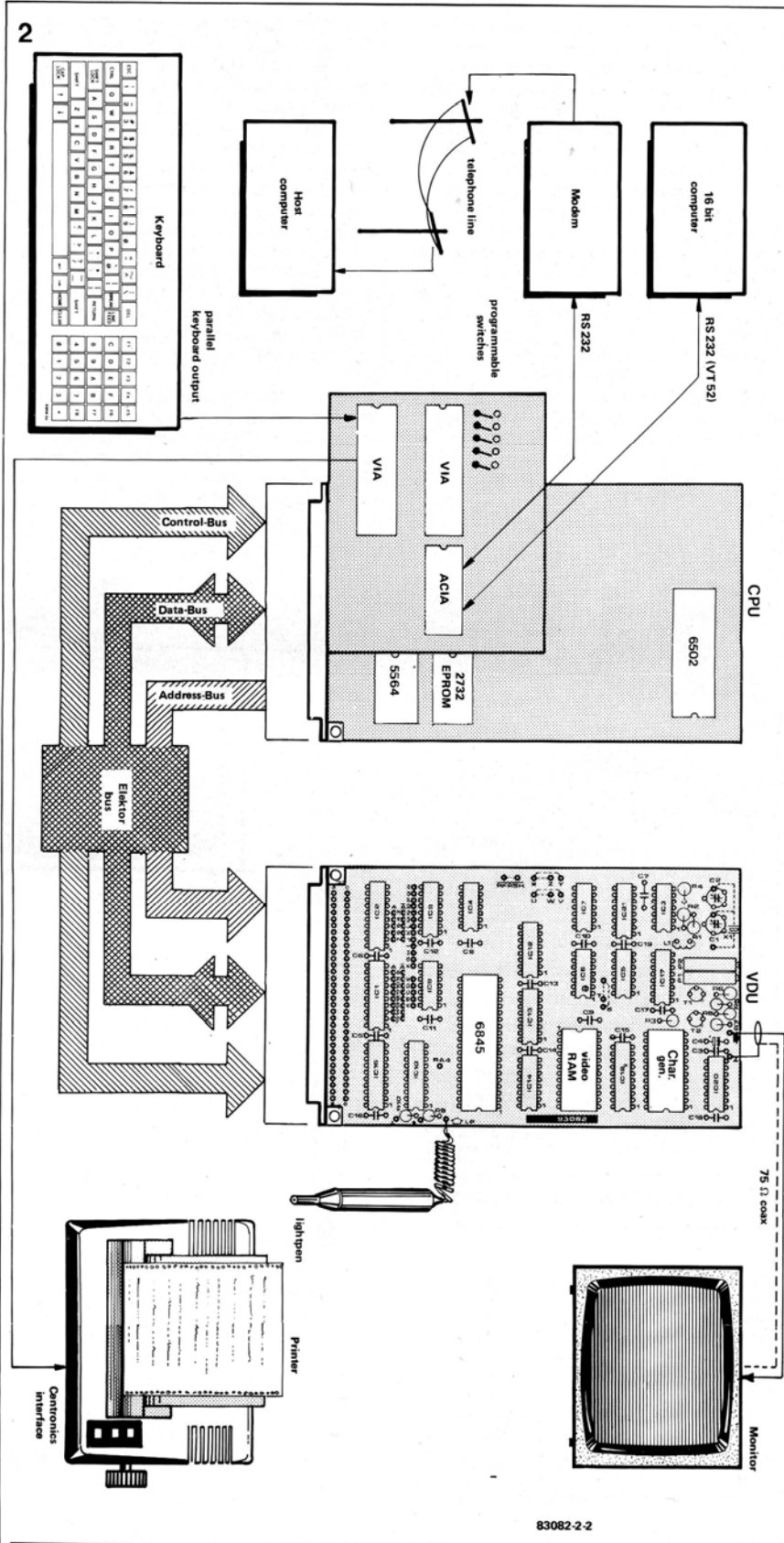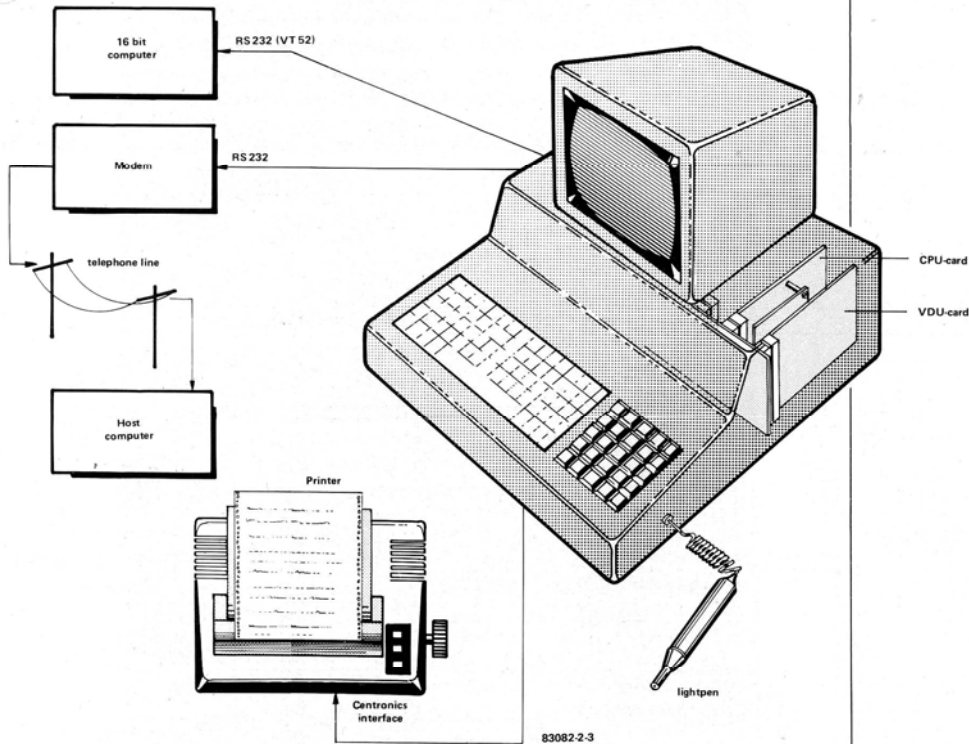
lightpen

Printer

Centronics
interface

75 Ω coax

Monitor

Figure 2. This shows what
can ultimately be achieved
with the universal terminal
containing a VDU card and
a CPU card. All the other
equipment (computer,
modem, printer, keyboard
and so on) can be con-
nected to this terminal.

83082-2-2

83082-2-3

possibilities with the VDU card but there are
even more to come. As a follow up to this
VDU card we will shortly publish a CPU
card especially developed to complement it.
These two cards will together form the basis
of a universal terminal with RS 232 interface
and VT 52 protocol, so that it can be con-
nected to virtually any computer. Figure 2
shows the main parts of this system and of
course this terminal can be connected to any
computer which has an RS 232 interface.
The CPU card contains a 6502 micropro-
cessor, 2 VIAs (Versatile Interface Adapter),
an ACIA (Asynchronous Communications
Interface Adapter) an EPROM and a RAM.
Thanks to a set of through connections on
the board the transfer format, speed, num-
ber of start and stop bits and the type and
number of control bits can be adapted to
whatever computer is connected to the
terminal. Similarly there is a choice of eight
different screen-image formats.
All that is needed to make up a complete
terminal is a VDU card, a CPU card, a
monitor and a keyboard. The terminal could,
for example, communicate over the tele-
phone lines via a modem, with a computer
in some other part of the globe, but because
of its VT 52 protocol it could also be con-
nected directly to a 16 bit computer. A
connection for a printer is, of course,
provided. It is also possible to use the CPU
card and VDU card together as the basis for
a complete computer system, as figure 3
shows. This example is connected to a 16

bitter but, in principle, that could be any
type of computer.
The terminal software is located in a 2716
EPROM on the CPU card which can have a
maximum of 8 K of random access memory
and 16 K of read only memory.
Clearly there are already quite a few possi-
bilities for this two-card combination and
certainly there are more than we have men-
tioned. However we will leave it at that until
the article on the CPU card.

The VDU card in a nutshell

Figure 4 shows the circuit diagram for the
VDU card. At the left is the system bus and
here we see that address lines A0 . . . A10
are connected to the B inputs of the 2 into 1
multiplexers, IC12 . . . IC14. Also address
lines A3 . . . A15 are inverted by N1 . . . N13.
Complete address decoding is thus possible
because the addresses are available either
normally at points A3 . . . A15 or inverted
at points $\overline{A}3$ . . . $\overline{A}15$. Address decoding for
the video RAM is carried out via N37, and
for the CRTC via N38. The numbers beside
these two gates refer to those used with the
Junior Computer. In this case the video
RAM is in the range D000 . . . D7FF and the
CRTC is between D800 and D80F.
When N37 gives a chip-select signal the video
RAM (IC15) is addressed from the system
bus by the microprocessor. By this the
address inputs of the 6116 are connected
to the address bus of the system via the A
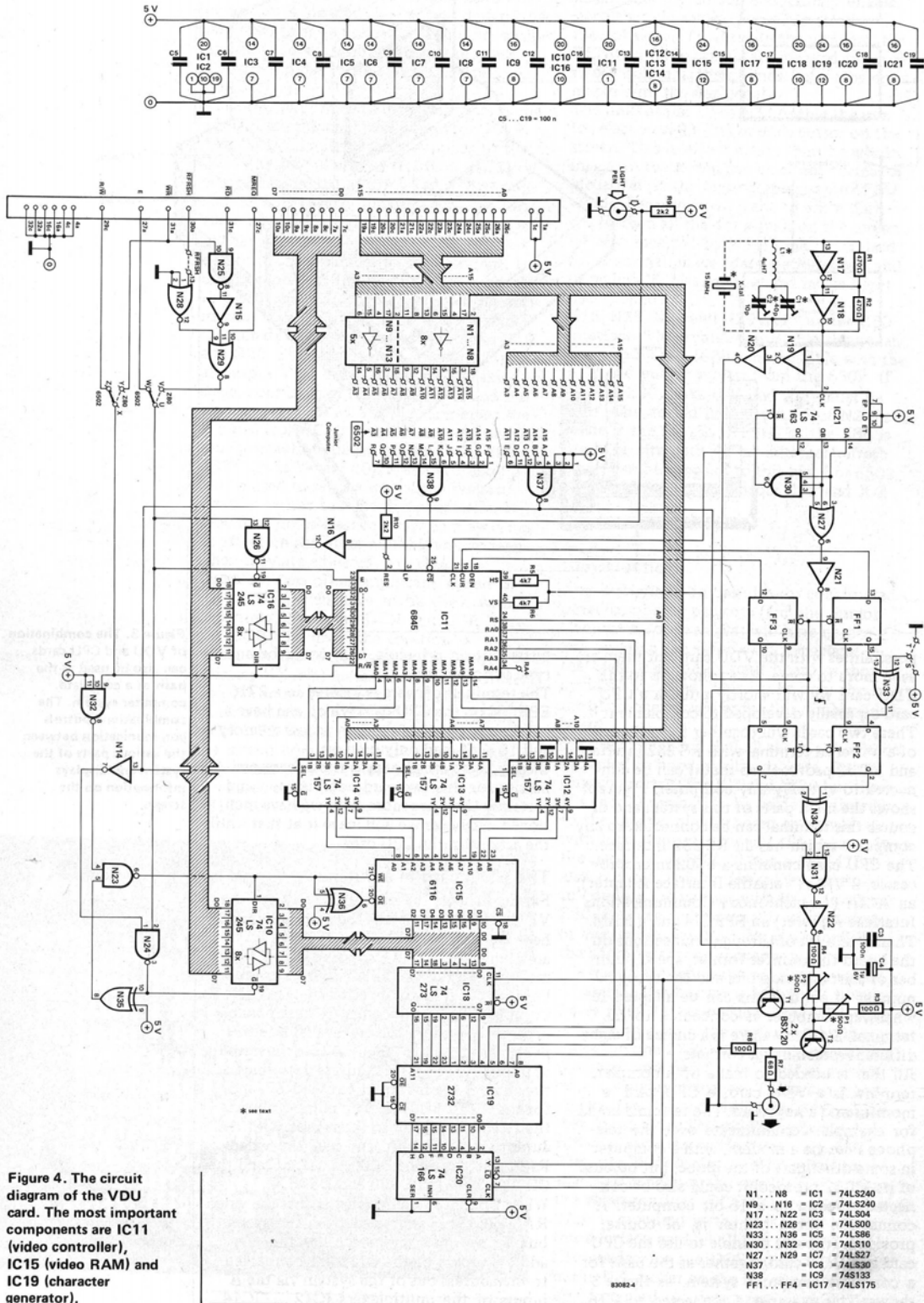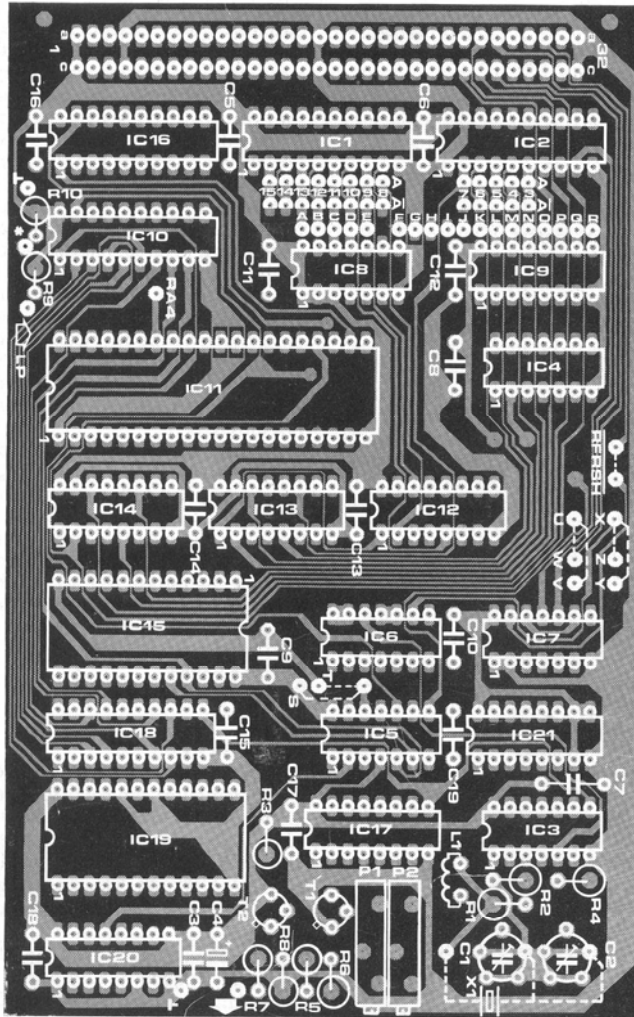inputs of the multiplexers IC12 . . . IC14

Figure 4. The circuit
diagram of the VDU
card. The most important
components are IC11
(video controller),
IC15 (video RAM) and
IC19 (character
generator).

N1 . . . N8	= IC1	= 74LS240
N9 . . . N16	= IC2	= 74LS240
N17 . . . N22	= IC3	= 74LS04
N23 . . . N26	= IC4	= 74LS00
N33 . . . N36	= IC5	= 74LS86
N30 . . . N32	= IC6	= 74LS10
N27 . . . N29	= IC7	= 74LS27
N37	= IC8	= 74LS30
N38	= IC9	= 74S133
FF1 . . . FF4	= IC17	= 74LS175

C5 . . . C19 = 100 n

83082-4

5

Figure 5. The component
layout for the VDU card.

(select inputs of the multiplexers are logic zero). At the same time data bus buffer IC10 is enabled via N14 and N24. The logic level of the R/W̄ line (pin 29c of the connector) ensures that IC15 is enabled via N32, N23 and the W̄Ē input.
If the CRTC is addressed from the system bus N38 gives a logic zero to the C̄S̄ input. The processor then has access to the internal registers of the 6845 via the system bus. Data bus buffer IC16 is then also enabled via N16 and N26.
IC16 is really only needed of a light pen is to be used with the VDU card. If this is not the case, and data is only written from the bus to the CRTC, then IC16 is superfluous and the 6845 can be connected directly to the data lines with eight wire links.
Address decoder N37 resets flip-flops FF1 . . . FF4 so that no rubbish appears on the screen when the processor accesses the video RAM.

The timing of the VDU card is controlled by the oscillator based on N17 and N18. This supplies the so-called dot frequency, which is 15 MHz for the screen format used here. A coil is necessary to maintain stability of the oscillator at this relatively high frequency. For optimum performance, a 15 MHz crystal could be used in the oscillator in place of C1, C2 and L1. IC21 divides the oscillator signal by eight. This IC is a synchronous counter which is reset via N30 when the count reaches seven. Because the reset is only processed by the IC on the following clock pulse, the IC then effectively counts to eight. Output QC delivers the character frequency for the controller. The CRTC counts continuously from ØØØ to 7FF (the whole range of the video RAM) at the frequency of this signal. As the processor now has no access to the video RAM, the address outputs MA0 . . . MA10 of IC12 are connected to the address inputs of the 6116

via the multiplexers, so that all the RAM addresses are continually accessed. The RAM then continuously supplies data which is placed into latch IC18. A latch is needed to enable the RAM to get all the data stable on the outputs, and it is not clocked until this condition is fulfilled. The output data of the latch can then be used while simultaneously another address is supplied to the RAM. The clock pulse for the latch is supplied via N21.

The information in the latch now acts as the address for the character generator, IC19. The CRTC simultaneously supplies to the 2732 the row addresses (RA0 . . . RA3) of every character to be displayed so that one row of dots is read out each time for the video line that is to be written on the screen at that time. IC20 converts the dot information from a parallel to serial format. In order to prevent timing faults from occurring with the high frequencies used the shift register is synchronous, and its clock signal is taken directly from the oscillator via N19 and N20. The serial dot information appears at output Y of the IC. The video mixing stage, consisting of N34, N31, N22 and the circuitry around T1 and T2, combines the Y signal from IC20 with the line and raster synchronization pulses supplied by the CRTC (pins 39 and 40). Presets P1 and P2 can be used to set the size of the synchronization pulses and the dot amplitude. It should be noted that each of the presets has an effect on the other and this will be seen when they are adjusted.

There are two other important signals of the CRTC which have to be dealt with separately. These are DEN and CUR. Output CUR(sor) gives the location of the cursor on the screen and output DEN (Display ENable) indicates when the CRTC is in the active range of the screen (see the section on 'image building' in the descriptive article). The latter signal is needed to keep the screen completely dark outside the active range. These two signals must now be combined with the video signal (via N34 and N31), but that cannot be done directly

because of the time that elapses between an address being supplied to the RAM and the appearance of the dot information at the outputs of the EPROM. The delay time is a few hundred nanoseconds, and that would mean that the cursor and display enable signals would appear too early relative to the dot signal. To alleviate the problem, the DEN and CUR signals are delayed by the two whole character times before being mixed with the dot signal.

The links at pin 12 of N33 enable the user to select a bright (lit) or dark cursor on the screen. This in effect means that the whole image on the screen can be either normal or 'negative' (in the photographic sense of the word), because if we want to use a dark cursor then all the dot signals on the screen are also inverted by N34. Link 'T' is used for a normal image (dark background) and using link 'S' gives an inverted image (light background).

N15, N25, N28 and N29 make up the Z80 interface. These gates ensure that the signals supplied by the Z80 are compatible with the R/W and enable signals from the 6502. If using a Z80, links U-V and X-Y must be used. The dotted link at pin 13 of N28 is made if the refresh ($\overline{\text{RFSH}}$) of the Z80 is used, or alternatively an external refresh signal can be supplied to this pin. For 6502 and 6800 family processors U-W and X-Z must be linked.

Construction

Any hobbyist who has already constructed other computer projects (for the Junior Computer, for example) will have no problem building the video card, especially if the Elektor printed circuit board as shown in figure 5 is used. This figure only shows the component overlay for this double sided board.

It is recommended that all the ICs should be mounted in good quality sockets. This is quite important for IC3 and IC20 but these ICs should preferably be soldered directly to the printed circuit board as they deal with high frequency signals. T1 is given in the parts list as BSX 20 but a BC 547B is also suitable. It is important to remember to connect the various wire links (in the Z80 interface and the one to select normal or inverted image), and the same applies for the address decoder connections.

If a crystal is used in the oscillator then L1, C1 and C2 can be omitted from the board. Three EPROMs are needed if the VDU card is to be used with the expanded Junior. These are one 2732 containing the character generator and two 2716s, TMV and PMV, with the video routines. These last two replace the TM and PME EPROMs and, as they contain the TM and PM software, the Junior is none the worse for it.

With the DOS Junior a 2732 with the character generator and one 2716 containing the video routines (DOSVT) are used. The 2716 is mounted in the socket for IC5 on the interface card. A CMOS RAM 6116 is also needed for the DOS Junior and is put in the IC4 socket on the interface card. This interface card requires a few modifications

```
Ok
RUN"BEXEC*

OS-65D Tutorial disk five - Sept. 16, 1981
 1 > Directory
 2 > Create a new file
 3 > Change a file name
 4 > Delete file from diskette
 5 > Create blank data diskette
 6 > Create data diskette with files
 7 > Create buffer space for data files
 8 > Single or dual disk drive copier
 9 > Enter OS-65D system
Type the number of your selection
and depress RETURN ?
```

for correct operation with the VDU card, so:
— pin 18 of IC4 is joined to pin 20
— the following connections are made: M-J, G-I, I'-G', J'-L', O'-M'.

The DOS Junior (unlike the expanded JC) requires a few software changes in order to work correctly with the VDU card. For this a V 3.3 diskette suitable for the Junior and an Elekterminal or another serial I/O device are needed.

First of all a copy of the diskette is made via Utility 8 and this copy is placed in drive A. Now the modifications given in table 1 are made and the following is entered on the Junior keyboard:

\<RST\>
\<AD\> A200
\<DA\>

and the bootstrap modifications from table 2 are given. This is followed by:

\<AD\> A311
\<DA\> FFFF (video output 1)
FFFF (video output 2)
A2FE (serial output 1)
E1F3 (Centronics output 1)

and then carry on with table 3. When that is done we then have a new V 3.3 diskette adapted to the VDU card.

If there is sufficient interest, we will possibly publish a Paperware to deal with this subject in greater depth, especially as regards the

operation of the CRTC and the associated software.

The EPROMs are available as a pre-programmed set from Technomatic Ltd-ESS 522 is for the expanded Junior and ESS 521 for the Junior with DOS.

The circuit works from a single supply of 5 V and draws a current of about 450 mA. When the power is switched on the system must be initialized by pressing the reset button. To set P1 and P2, these two presets are first put to their mid positions. Then they are adjusted to get a clear image on the screen. If a TV set is used instead of a monitor the contrast control must be turned back completely as the bandwidth is generally too large. Trimmers C1 and C2 are used to set the frequency so that the image remains stable on the screen. If a 15 MHz crystal is used in the oscillator this last adjustment is unnecessary. ◀

Table 1.

AXCA 0200 = 39,1

AXCA 2000 = 39,2

AXGO 0200

— DISKETTE UTILITIES —

SELECT ONE:
1) COMPAR
2) TRACK 0 READ/WRITE
? 2

— TRACK ZERO READ/WRITE UTILITY —

COMMANDS:
Rnnnn — READ INTO LOCATION nnnn
Wnnnn/9999,P — WRITE FROM nnnn FOR p PAGES
WITH 9999 AS THE LOAD VECTOR
3 — EXIT TO OS-65D

COMMAND: RA 200

— TRACK ZERO READ/WRITE UTILITY

COMMANDS:
Rnnnn — READ INTO LOCATION nnnn.
Wnnnn/9999,P — WRITE FROM nnnn FOR p PAGES
WITH 9999 AS THE LOAD VECTOR
E — EXIT TO OS-65D

COMMAND? E

AXCA AA00 = 01,1

AX

Table 1. This is how track 0 of the floppy disk is transferred to the RAM memory starting at address \$A200 and track 1 to RAM starting at address \$AA00.

Table 2.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
A200 :	A9	01	8D	5E	26	20	BC	26	A9	2A	85	FF	20	54	27	86
A210 :	FE	20	67	29	20	79	2E	A0	BF	20	EC	22	F0	03	88	D0
A220 :	F8	8C	00	23	A2	01	8E	C6	2A	4C	41	22	EA	EA	EA	EA
A230 :	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA	EA
A240 :	EA	A9	00	8D	F7	EF	8D	D2	EF	20	35	F4	20	30	F3	20
A250 :	61	27	20	73	2D	0D	0A	0A	2A	44	4F	53	20	4A	55	4E
A260 :	49	4F	52	20	43	4F	4D	50	55	54	45	52	20	20	56	32
A270 :	2E	30	2A	0D	0A	0A	43	4F	50	59	52	49	47	48	54	20
A280 :	42	59	20	45	4C	45	4B	54	4F	52	00	A9	2E	8D	7C	FA
A290 :	A9	FF	8D	7D	FA	A9	00	8D	7A	FA	A9	FC	8D	7B	FA	4C
A2A0 :	E6	2A														

Table 2. This is the data needed to modify the bootstrap section.

Table 3.

AXGO 0200

— DISKETTE UTILITIES —

SELECT ONE:
1) COMPAR
2) TRACK 0 READ/WRITE
? 2

— TRACK ZERO READ/WRITE UTILITY —

COMMANDS:
Rnnnn — READ INTO LOCATION nnnn.
Wnnnn/9999,P — WRITE FROM nnnn FOR p PAGES
WITH 9999 AS THE LOAD VECTOR
E — EXIT TO OS-65D

COMMAND? WA 200/2200,8

— TRACK ZERO READ/WRITE UTILITY —

COMMANDS:
Rnnnn — READ INTO LOCATION nnnn.
Wnnnn/9999,P — WRITE FROM nnnn FOR p PAGES
WITH 9999 AS THE LOAD VECTOR
E — EXIT TO OS-65D

COMMAND? E

AXSA 01,1 = AA00/8

AX

Table 3. Here we see how the modified bootstrap is written back to the floppy disk.